REMARKS

Claims 4-82 are pending in this application. Claims 4-7, 9, 29, 36-42, 53, and 82 have been rejected. Claims 84-108 have been withdrawn from consideration. Claims 8, 10-28, 30-35, 43-52, and 54-81 have been allowed. Claim 4 has been amended.

A restriction under 35 U.S.C. § 121 has been made to one of two inventions: Group I, claims 4-82, drawn to a memory device having a reference cell, and Group II, claims 84-108, drawn to a memory device including a spare (or redundant) array. Applicant affirms the provisional election without traverse to prosecute the invention of Group I, claims 4-82. Applicant notes that claims 84-108 have been withdrawn from further consideration by the Examiner, as being drawn to a nonelected invention.

Claims 4-7, 9, 29, 36-42 and 53, have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claim 4 has been rejected for being indefinite with respect to the "at least one memory decoder" in the second paragraph and the third paragraph. Claim 4 has been amended to delete the third paragraph for at least one memory decoder, which was erroneously included in the clean copy of the claims. Therefore, it is respectfully submitted that claim 4 and claims 5-7, 9, 29, 36-42 and 53 which depend on claim 4, are not indefinite, and withdrawal of the section 112 rejection is respectfully submitted.

Claims 4-5, 7, 9, 29, 36-39, 53 and 82 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Tsen* (U.S. Patent No. 5,936,906).

Claim 4 has been amended merely to correct the § 112 rejection as described above. Claim 4 recites the plurality of multidimensional segmented memory arrays.

Tsen at best merely discloses a primary cells array 100 that includes flash cells that store multilevel digital data. A word decoder 102 selects flash cells using word lines WL. A bitline decoder 104 selects bitlines BL connected to the flash cells. ('906 patent, col.2, ln.60-col3, ln.5.) "[A] reference cells array 110 is electrically coupled to the primary cells array 100 via the word lines [WL] for sharing the word lines [WL]." ('906 patent, col.3, lns. 6-8.) The reference latch cells are set at threshold voltages by applying reference signals to the corresponding word line that is selected by the word line decoder 102. ('906 patent, col.3, ln.66-col.4, ln.16.) During reads from the memory cells, the current from the read memory cell is compared in the sense

amplifier 120 to the reference currents stored in the reference cells array 110. ('906 patent, col.4, lns.38-59.)

Figure 3 of *Tsen* shows an example of a primary cells array 100 that includes eight flash cells M1-M8 that each store 3 bits of digital data. ('906 patent, col. 3, lns. 39-41.) The common line S1 or S2 connect source terminals of a column of memory cells. In this arrangement, all cells in a column or all cells in a word row are enabled by bit lines or word lines, respectively. Likewise, Figure 4 of *Tsen* shows the reference cells array 110 that are similarly arranged as the primary cells array 100.

In contrast, the memory arrays of claim 4 are segmented memory. Segmented arrays can be operated on while memory cells in unselected segments are unselected.

As an illustrative example, reference is made to segmented arrays shown in Figures 3C and 4A-4E of the Specification. As shown in the segmented array of Figure 4A, the segmented array includes columns that are coupled by segmented bitlines SBL0 through SBL7. These bitlines are separately decoded to allow isolation and inhibiting of unselected columns in the segment and other segments. For example, the cells coupled to segmented bitline SBL0 are selected while the cells coupled to the segmented bit line SBL1 are not selected, and these two segmented bitlines SBL0 and SBL1 are coupled to the bitline BLP0 240. In these embodiments, while a selected segmented array is then accessed, all other segmented arrays may be deselected so that all terminals of the memory cells of the unselected segments are unselected. Thus as shown in Figure 4A of the specification, the cells are the segmented bit line SBL0 are accessed while the cells on the segmented bit lilne SBL1 are inhibited and other segmented arrays are inhibited.

It is asserted that Figure 4 of *Tsen* shows memory cells connecting bit lines BL1 and BL2 and word lines WL1-WL4 as one segmented memory array and the memory cells connected to bit lines BL3 and BL4 and the word lines WL1-WL4 as another segmented memory array. Applicant respectfully disagrees with this assessment of Figure 4 of *Tsen*. In Figure 4 of *Tsen*, if word line 1 is enabled, all memory cells connected to the word line WL1 are enabled whether connected to bit lines BL1, BL2 or BL3. In contrast, in the array segments 290 as found in Figure 3C of the Specification and various embodiments of the array segments as shown in Figures 4A-4F, each segment array segment 290 is addressed separately, and addressing within the segmented array allows cells to be unselected, such as the example noted above for

segmented bitlines SBL0 and SBL1. This allows the array to be addressed in segments and not enable entire rows or columns of an array. *Tsen* does not disclose or even suggest multidimensional segmented memory arrays as recited in amended claim 4.

Lacking the disclosure of this claim feature, *Tsen* cannot render claim 4 unpatentable. Because claims 5-7, 36-42, and 53 depend, directly or indirectly, on claim 4, for similar reasons claims 5-7, 36-42 and 53 are not rendered unpatentable by *Tsen*. Therefore, it is respectfully submitted that claims 4-7, 36, 42 and 53 are patentable over the references of record.

Claim 82 recites in pertinent part 'a plurality of segmented memory arrays". As described above *Tsen* does not disclose or even suggest segmented memory arrays as recited in claim 82. Lacking the disclosure of this claim feature, *Tsen* cannot render claim 82 unpatentable. Therefore, it is respectfully submitted that claim 82 is patentable over the references of record.

Claims 40-42 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Tsen* in view of *Banks* (U.S. Patent No. 6,602,614). This rejection is respectfully traversed.

As described above, *Tsen* does not disclose multidimensional segmented memory arrays. *Banks* at best merely discloses a multibit per cell electrically alterable non-volatile memory system 100 that includes an MxN array of non-volatile cells. Word lines 104 connect the memory cells. Bitlines 106 connect columns of memory cells. The output of sense amplifiers 112 coupled to the bitlines and a reference voltage detect a voltage. A decode/encode circuit 114 decodes the data bits which are latched in an input/output, N-bit latch/buffer 116. ('614 patent, Fig.5, col.8, l.43-col.9, l.7). The memory cells are not arranged in segmented arrays for the same reasons described above for *Tsen*. The array of *Banks* is not a multidimensional segmented memory array, but a single array.

Neither *Tsen* nor *Banks*, either individually or in combination, disclose or even suggest a plurality of multidimensional segmented memory arrays as recited in claim 4, or in claims 40-42, which depend on claim 4, and thus cannot render claims 40-42 unpatentable.

Therefore, it is respectfully submitted that claims 40-42 are patentable over the references of record.

The allowance of claim 8, 10-28, 30-35, 43-52, and 54-81 is noted.

It is submitted that claims 4-82 are allowable, and allowance and issuance of this application is respectfully requested.

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